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PETITION FOR REVIVAL OF AN APPLICATION FOR PATENT ABANDONED UNAVOIDABLY UNDER 37 CFR 1.137(a)

Docket Number (Optional): 0553-0163

First Named Inventor: Satoshi Murakami

Art Unit: 2815

Application Number: 09/516,082

Examiner: Eugene Lee

Filed: March 1, 2000

Title: Semiconductor Device and Method of Manufacturing the Same

Attention: Office of Petitions
Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

NOTE: If information or assistance is needed in completing this form, please contact Petitions Information at (703) 305-9382.

The above-identified application became abandoned for failure to file a timely and proper reply to a notice or action by the United Sates Patent and Trademark Office. The date of abandonment is the day after the expiration date of the period set for reply in the Office notice or action plus any extensions of time actually obtained.

APPLICANT HEREBY PETITIONS FOR REVIVAL OF THIS APPLICATION.

NOTE: A grantable petition requires the following items:

(1) Petition fee.
(2) Reply and/or issue fee.
(3) Terminal disclaimer with disclaimer fee-required for all utility and plant applications filed before June 8, 1995, and for all design applications; and
(4) Adequate showing of the cause of unavoidable delay.

1. Petition fee

☐ Small entity – fee $_____ (37 CFR 1.17(l)). Applicant claims small entity status. See 37 CFR 1.27.

☒ Other than small entity – fee $ 110.00 (37 CFR 1.17(l)).

2. Reply and/or fee

A. The reply and/or fee to the above-noted Office action in the form of Amendment E - After Final, IDS, RCE & Check for $1,958.00 (identify the type of reply):

☒ has been filed previously on February 3, 2004.

☒ is enclosed herewith (with the correct serial number).

B. The issue fee of $ _____

☐ has been filed previously on _____.

☐ is enclosed herewith.

PETITION FOR REVIVAL OF AN APPLICATION FOR PATENT ABANDONED UNAVOIDABLY UNDER 37 CFR 1.137(a)

3. Terminal disclaimer with disclaimer fee

☐ Since this utility/plant application was filed on or after June 8, 1995, no terminal disclaimer is required.

☐ A terminal disclaimer (and disclaimer fee (37 CFR 1.20(d)) of $ _____ for a small entity or $ _____ for other than a small entity) disclaiming the required period of time is enclosed herewith (see PTO/SB/63).

4. An adequate showing of the cause of the delay, and that the entire delay in filing the required reply from the due date for the reply until the filing of a grantable petition under 37 CFR 1.137(a) was unavoidable, is enclosed.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

June 30, 2004
Date

Stephen B. Heller
Signature

312-236-8500
Telephone Number

Stephen B. Heller
Typed or printed name

30,181
Registration Number, if applicable

200 West Adams, Suite 2850
Address

Chicago, Illinois 60606
Address

Enclosure
☒ Fee Payment
☒ ~~Reply~~ - Amendment E, Information Disclosure Statement and Request for Continued Examination
☐ Terminal Disclaimer Form
☒ Additional sheets containing statements establishing unavoidable delay
☐ _____

CERTIFICATE OF MAILING OR TRANSMISSION (37 CFR 1.8(a))

I hereby certify that this correspondence is being:

☒ deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to **Mail Stop Petition**, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

☐ transmitted by facsimile on the date shown below to the United States Patent and Trademark Office at (703) 872-9306.

June 30, 2004
Date

Christine A. Barglik
Signature

Christine A. Barglik
Typed or printed name of person signing certificate

PTO/SB/61 (11-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PETITION FOR REVIVAL OF AN APPLICATION FOR PATENT ABANDONED UNAVOIDABLY UNDER 37 CFR 1.137(a)

NOTE: The following showing of the cause of unavoidable delay must be signed by all applicants or by any other party who is presenting statements concerning the cause of delay.

June 30, 2004	Stephen B. Heller
Date	Signature
30,181	Stephen B. Heller
Registration Number, if applicable	Typed or printed name

(In the space provided below, please explain in detail the reasons for the delay in filing a proper reply.)

(Please attach additional sheets if additional space is needed.)

PATENT
Attorney Docket No. 0553-0163

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Satoshi Murakami, et al.

Serial No: 09/516,082

Filed: March 1, 2000

Art Unit: 2815

Examiner: Eugene Lee

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DATE: June 30, 2004

NAME: Christine A. Barglik

SIGNATURE: Christine A. Barglik

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REASONS FOR DELAY IN FILING THE RESPONSE

An Office Action mailed December 3, 2003 making a final rejection of the pending claims was received on December 8, 2003 and was properly docketed for response (3 month) for March 3, 2004.

On February 3, 2004 a response to the Office Action, namely Amendment E - After Final, was filed along with a Request for Continued Examination, an Information Disclosure Statement, and a check in the amount of $1,958.00. Copies of these documents are attached hereto as Exhibit 1.

The return postcard indicating receipt of the materials by the Patent Office on February 6, 2004, was received on February 12, 2004. A copy of the postcard is attached as Exhibit 2.

On June 17, 2004 Mark Murphy, one of the attorneys responsible for prosecuting the application, received a telephone call from Examiner Lee inquiring as to whether a response had been filed with respect to the Office Action of December 3, 2003.

At this time, it was determined that in the documents filed by mail on February 3, 2004, the final two numbers of the application's serial number were transposed. Specifically, the application number was listed as 09/516,028. It should have indicated the serial number to be 09/516,082.

Accordingly, even though a full response had been filed in a timely manner, it was not determined that the filing was ineffective to respond to the Office Action until having received a phone call from the Examiner.

Respectfully submitted,

Dated: June 30, 2004

Stephen B. Heller
Registration No.: 30,181

COOK, ALEX, McFARRON, MANZO,
CUMMINGS & MEHLER, LTD.
200 West Adams Street, Suite 2850
Chicago, Illinois 60606
(312) 236-8500

PATENT
Attorney Docket No. 0553-0163

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:)
)
Satoshi Murakami, et al.)
)
Serial No: 09/516,028)
)
Filed: March 1, 2000)
)
Art Unit: 2815)
)
Examiner: Eugene Lee)
)
For: SEMICONDUCTOR DEVICE)
AND METHOD OF)
MANUFACTURING THE SAME)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on February 3, 2004

Signature: [signature]

Date February 3, 2004

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT E - AFTER FINAL

Dear Sir:

In response to the Office Action dated December 3, 2003, please amend the above-identified application as follows.

IN THE CLAIMS:

Please amend the following claims 46-88 as follows.

1-45. (Canceled)

46. (previously presented) A semiconductor device comprising:

a first thin film transistor formed over an insulating surface, the first thin film transistor comprising:

a semiconductor film comprising crystalline silicon and having at least source and drain regions and a channel forming region;

a gate insulating film over the channel forming region; and

a gate electrode formed over the gate insulating film;

an interlayer insulating film formed over the first thin film transistor;

a conductive layer formed over the interlayer insulating film and electrically connected to one of the source and drain regions of the first thin film transistor;

a color filter having a flattened surface formed over the interlayer insulating film and the conductive layer; and

a pixel electrode formed over the color filter and electrically connected to the conductive layer.

47. (previously presented) A semiconductor device comprising:

a first thin film transistor formed over an insulating surface, the first thin film transistor comprising:

a semiconductor film comprising at least a channel forming region;

a gate insulating film adjacent to the channel forming region; and

a gate electrode adjacent to the gate insulating film,

an interlayer insulating film formed over the first thin film transistor;

a conductive layer formed over the interlayer insulating film and electrically connected to one of source and drain regions of the first thin film transistor;

a color filter having a flattened surface formed over the interlayer insulating film and the conductive layer; and

a pixel electrode formed over the color filter and electrically connected to the conductive layer.

48. (previously presented) A semiconductor device comprising:

a first thin film transistor formed over an insulating surface, the first thin film transistor comprising:

a semiconductor film comprising crystalline silicon and having at least source and drain regions and a channel forming region;

a gate insulating film adjacent to the channel forming region; and

a gate electrode adjacent to the channel forming region with the gate insulating film interposed therebetween;

an interlayer insulating film formed over the first thin film transistor, the interlayer insulating film comprising at

least a material selected from the group consisting of silicon nitride, silicon oxide and nitrated silicon oxide;

a color filter having a flattened surface formed over the interlayer insulating film; and

a pixel electrode formed over the color filter,

wherein the pixel electrode is electrically connected to the first thin film transistor.

49. (previously presented) A device according to claim 48, wherein the gate electrode is located over the channel forming region.

50. (previously presented) A semiconductor device comprising:

a first thin film transistor formed over an insulating surface, the first thin film transistor comprising:

a semiconductor film comprising silicon and having at least a channel forming region;

a gate insulating film adjacent to the channel forming region; and

a gate electrode adjacent to the channel forming region with the gate insulating film interposed therebetween;

an interlayer insulating film formed over the first thin film transistor, the interlayer insulating film comprising at least a material selected from the group consisting of silicon nitride, silicon oxide and nitrated silicon oxide;

a color filter having a flattened surface formed over the interlayer insulating film; and

a pixel electrode formed over the color filter.

51. (previously presented) A device according to claim 50, wherein the gate electrode is located over the channel forming region.

52. (previously presented) A semiconductor device comprising:

a first thin film transistor formed over an insulating surface, the first thin film transistor comprising:

a semiconductor film comprising crystalline silicon and having at least source and drain regions and a channel forming region;

a gate insulating film adjacent to the channel forming region; and

a gate electrode formed adjacent to the channel forming region with the gate insulating film interposed therebetween;

a first interlayer insulating film formed over the first thin film transistor;

a conductive layer formed over the first interlayer insulating film and electrically connected to one of the source and drain regions of the first thin film transistor;

a passivation film formed over the conductive layer, the passivation film comprising at least a material selected from the group consisting of silicon nitride, silicon oxide and nitrated silicon oxide;

a color filter having a flattened surface formed over the passivation film; and

a pixel electrode formed over the color filter and electrically connected to the conductive layer.

53. (previously presented) A device according to claim 52, wherein the gate electrode is located over the channel forming region.

54. (previously presented) A semiconductor device comprising:

a first thin film transistor formed over a substrate, the first thin film transistor comprising:

a semiconductor film comprising silicon and having at least a channel forming region;

a gate insulating film adjacent to the channel forming region; and

a gate electrode adjacent to the channel forming region with the gate insulating film interposed therebetween;

a first interlayer insulating film formed over the first thin film transistor;

a conductive layer formed over the first interlayer insulating film and electrically connected to one of the source and drain regions of the first thin film transistor;

a passivation film formed over the conductive layer, the passivation film comprising at least a material selected from the group consisting of silicon nitride and nitrated silicon oxide;

a color filter having a flattened surface formed over the passivation film; and

a pixel electrode formed over the color filter and electrically connected to the conductive layer.

55. (previously presented) A device according to claim 54, wherein the gate electrode is located over the channel forming region.

56. (previously presented) A semiconductor device comprising:

a first thin film transistor formed over an insulating surface, the first thin film transistor comprising:

a semiconductor film comprising :

a channel forming region; and

a source region and a drain region in contact with the LDD regions;

a gate insulating film adjacent to the channel forming region; and

a gate electrode adjacent to the gate insulating film;

an interlayer insulating film formed over the first thin film transistor;

a conductive layer formed over the interlayer insulating film and electrically connected to one of source and drain regions of the first thin film transistor;

a color filter formed over the interlayer insulating film, the conductive layer and the first thin film transistor; and

a pixel electrode formed over the color filter and electrically connected to the conductive layer.

57. (previously presented) A semiconductor device comprising:

a first thin film transistor formed over an insulating surface, the first thin film transistor comprising:

a semiconductor film comprising:

a channel forming region; and

a source region and a drain region in contact with the LDD regions;

a gate insulating film adjacent to the channel forming region; and

a gate electrode adjacent to the channel forming region with the gate insulating film interposed therebetween;

an interlayer insulating film formed over the first thin film transistor, the interlayer insulating film comprising at least a material selected from the group consisting of silicon nitride, silicon oxide and nitrated silicon oxide;

a color filter formed over the interlayer insulating film and the first thin film transistor; and

a pixel electrode formed over the color filter.

58. (previously presented) A semiconductor device comprising:

a first thin film transistor formed over an insulating surface, the first thin film transistor comprising:

a semiconductor film comprising:

a channel forming region; and

a source region and a drain region in contact with the LDD regions;

a gate insulating film adjacent to the channel forming region; and

a gate electrode adjacent to the channel forming region with the gate insulating film interposed therebetween;

a first interlayer insulating film formed over the first thin film transistor;

a conductive layer formed over the first interlayer insulating film and electrically connected to one of the source and drain regions of the first thin film transistor;

a passivation film formed over the conductive layer, the passivation film comprising at least a material selected from the group consisting of silicon nitride and nitrated silicon oxide;

a color filter formed over the passivation film and the first thin film transistor; and

a pixel electrode formed over the color filter and electrically connected to the conductive layer.

59. (previously presented) A semiconductor device comprising:

a first thin film transistor comprising:

a semiconductor film comprising at least a channel forming region;

a gate insulating film adjacent to the channel forming region; and

a gate electrode adjacent to the channel forming region with the gate insulating film interposed therebetween;

an interlayer insulating film formed over the first thin film transistor;

a conductive layer formed over the interlayer insulating film and electrically connected to one of source and drain regions of the first thin film transistor;

a color filter formed over the interlayer insulating film, the conductive layer and the first thin film transistor; and

a pixel electrode formed over the color filter and electrically connected to the conductive layer~~,~~

~~wherein the pixel matrix circuit and the driver circuit are over a same substrate~~.

60. (previously presented) A semiconductor device comprising:

a first thin film transistor comprising:

a semiconductor film comprising silicon and having at least a channel forming region;

a gate insulating film adjacent to the channel forming region; and

a gate electrode adjacent to the channel forming region with the gate insulating film interposed therebetween;

an interlayer insulating film formed over the first thin film transistor, the interlayer insulating film comprising at least a material selected from the group consisting of silicon nitride, silicon oxide and nitrated silicon oxide;

a color filter formed over the interlayer insulating film and the first thin film transistor; and

a pixel electrode formed over the color filter.

61. (previously presented) A semiconductor device comprising:

a first thin film transistor comprising:

a semiconductor film comprising silicon and having at least a channel forming region;

a gate insulating film adjacent to the channel forming region; and

a gate electrode adjacent to the channel forming region with the gate insulating film interposed therebetween;

a first interlayer insulating film formed over the first thin film transistor;

a conductive layer formed over the first interlayer insulating film and electrically connected to one of the source and drain regions of the first thin film transistor;

a passivation film formed over the conductive layer, the passivation film comprising at least a material selected from the group consisting of silicon nitride and nitrated silicon oxide;

a color filter formed over the passivation film and the first thin film transistor; and

a pixel electrode formed over the color filter and electrically connected to the conductive layer.

62. (previously presented) A device according to claim 56, wherein the semiconductor film comprises crystalline silicon.

63. (previously presented) A device according to claim 57, wherein the semiconductor film comprises crystalline silicon.

64. (previously presented) A device according to claim 58, wherein the semiconductor film comprises crystalline silicon.

65. (previously presented) A device according to claim 59, wherein the semiconductor film comprises crystalline silicon.

66. (previously presented) A device according to claim 60, wherein the semiconductor film comprises crystalline silicon.

67. (previously presented) A device according to claim 61, wherein the semiconductor film comprises crystalline silicon.

68. (Currently Amended) A device according to claim 46, wherein the semiconductor device further comprising:

a resin film over the color filter;

an electrode over the organic resin film; and

an oxide film of the ~~first~~ electrode in direct contact with at least a portion of a surface of the ~~first~~ electrode,

wherein the pixel electrode is in direct contact with at least a portion of the oxide film, and

wherein a storage capacitor comprises the electrode and the pixel electrode with the oxide film interposed therebetween.

69. (Currently Amended) A device according to claim 48, wherein the semiconductor device further comprising:

a resin film over the color filter;

an electrode over the organic resin film; and

an oxide film of the ~~first~~ electrode in direct contact with at least a portion of a surface of the ~~first~~ electrode,

wherein the pixel electrode is in direct contact with at least a portion of the oxide film, and

wherein a storage capacitor comprises the ~~first~~ electrode and the pixel electrode with the oxide film interposed therebetween.

70. (Currently Amended) A device according to claim 52, wherein the semiconductor device further comprising:

a resin film over the color filter;

an electrode over the organic resin film; and

an oxide film of the ~~first~~ electrode in direct contact with at least a portion of a surface of the ~~first~~ electrode,

wherein the pixel electrode is in direct contact with at least a portion of the oxide film, and

wherein a storage capacitor comprises the ~~first~~ electrode and the pixel electrode with the oxide film interposed therebetween.

71. (previously presented) A device according to claim 46, wherein the semiconductor film further comprises LDD regions between the channel forming region and the source and drain regions.

72. (previously presented) A device according to claim 48, wherein the semiconductor film further comprises LDD regions

between the channel forming region and the source and drain regions.

73. (previously presented) A device according to claim 52, wherein the semiconductor film further comprises LDD regions between the channel forming region and the source and drain regions.

74. (previously presented) A device according to claim 56, wherein the semiconductor film further comprises LDD regions between the channel forming region and the source and drain regions.

75. (previously presented) A device according to claim 57, wherein the semiconductor film further comprises LDD regions between the channel forming region and the source and drain regions.

76. (previously presented) A device according to claim 58, wherein the semiconductor film further comprises LDD regions between the channel forming region and the source and drain regions.

77. (previously presented) A device according to claim 46, further comprising a driver circuit comprising a second thin film transistor,

wherein the first thin film transistor is included in a pixel matrix circuit, and

wherein the pixel matrix circuit and the driver circuit are formed over an insulating surface.

78. (previously presented) A device according to claim 47, further comprising a driver circuit comprising a second thin film transistor,

wherein the first thin film transistor is included in a pixel matrix circuit, and

wherein the pixel matrix circuit and the driver circuit are formed over an insulating surface.

79. (previously presented) A device according to claim 48, further comprising a driver circuit comprising a second thin film transistor,

wherein the first thin film transistor is included in a pixel matrix circuit, and

wherein the pixel matrix circuit and the driver circuit are formed over an insulating surface.

80. (previously presented) A device according to claim 50, further comprising a driver circuit comprising a second thin film transistor,

wherein the first thin film transistor is included in a pixel matrix circuit, and

wherein the pixel matrix circuit and the driver circuit are formed over an insulating surface.

81. (previously presented) A device according to claim 52, further comprising a driver circuit comprising a second thin film transistor,

wherein the first thin film transistor is included in a pixel matrix circuit, and

wherein the pixel matrix circuit and the driver circuit are formed over an insulating surface.

82. (previously presented) A device according to claim 54, further comprising a driver circuit comprising a second thin film transistor,

wherein the first thin film transistor is included in a pixel matrix circuit, and

wherein the pixel matrix circuit and the driver circuit are formed over an insulating surface.

83. (previously presented) A device according to claim 56, further comprising a driver circuit comprising a second thin film transistor,

wherein the first thin film transistor is included in a pixel matrix circuit, and

wherein the pixel matrix circuit and the driver circuit are formed over an insulating surface.

84. (previously presented) A device according to claim 57, further comprising a driver circuit comprising a second thin film transistor,

wherein the first thin film transistor is included in a pixel matrix circuit, and

wherein the pixel matrix circuit and the driver circuit are formed over an insulating surface.

85. (previously presented) A device according to claim 58, further comprising a driver circuit comprising a second thin film transistor,

wherein the first thin film transistor is included in a pixel matrix circuit, and

wherein the pixel matrix circuit and the driver circuit are formed over an insulating surface.

86. (previously presented) A device according to claim 59, further comprising a driver circuit comprising a second thin film transistor,

wherein the first thin film transistor is included in a pixel matrix circuit, and

wherein the pixel matrix circuit and the driver circuit are formed over an insulating surface.

87. (previously presented) A device according to claim 60, further comprising a driver circuit comprising a second thin film transistor,

wherein the first thin film transistor is included in a pixel matrix circuit, and

wherein the pixel matrix circuit and the driver circuit are formed over an insulating surface.

88. (previously presented) A device according to claim 61, further comprising a driver circuit comprising a second thin film transistor,

wherein the first thin film transistor is included in a pixel matrix circuit, and

wherein the pixel matrix circuit and the driver circuit are formed over an insulating surface.

REMARKS

We are in receipt of the Office Action dated December 3, 2003, and the above amendment and the following remarks are made in light thereof.

Claims 46-88 are pending in the application. Pursuant to the Office Action, claims 46-88 are rejected. Specifically, claims 59, 65, 68 and 86 are rejected under 35 USC 112 for indefiniteness due to a lack of antecedent basis for certain language in claims 59 and 68. Claims 46, 47, 56 and 62 are rejected under 35 USC 102(e) as being anticipated by Kadota et al. 5,818,550. Claims 48-55, 57, 58, 60, 61, 63, 64, 66 and 67 stand rejected under 35 USC 103 as being unpatentable over Kadota et al. and further in view of Seo 6,323,521. Claims 71, 73, and 74 are rejected under 35 USC 103 as being unpatentable over Kadota et al. and further in view of Ha 5,677,207. Claims 72, 75 and 76 stand rejected under 35 USC 103 as being patentable over Kadota et al. in view of Seo and further in view of Ha. Claims 77, 78, 83 and 86 are rejected under 35 USC 103 for being unpatentable over Kadota et al. further in view of Matsumoto 5,323,042. Claims 79-82, 84, 85, 87 and 88 stand rejected under 35 USC 103 as being unpatentable over Kadota et al. in view of Seo and further in view of Matsumoto. Claim 68 stands rejected under 35 USC 103 as being unpatentable over Kadota et al. further in view of Mikoshiba 5,499,123. Claims 69 and 70 stand rejected under 35 USC 103 as being unpatentable

over Kadota et al. in view of Seo and further in view of Mikoshiba. These rejections are made final.

Turning first to the rejections for indefiniteness. Claims 59 and 68 have been amended to address the examiner's rejection. Additionally, claims 69 and 70 have been amended for similar reasons as apply to claim 68.

Turning to the rejections based upon prior art, all of the pending independent claims, except for claim 59 (which has not been rejected based upon prior art), are rejected over Kadota et al. either alone or in view of one or more of Seo, Ha, Matsumoto, and Mikoshiba.

Turning first to independent claims 46-48, 50, 52, and 54, a color filter is required that has a flatten surfaced formed over the interlayer insulating film and the conductive layer. The examiner contends that Kadota et al. which is a color filter having a flattened surface. The examiner identifies color filters 9R/9G/9B, which are shown in Fig. 1. In addition, the specification for Kadota et al. states, at Col. 4, lines 31-35: "The second layer is overlain by a third layer which is constituted by a planarization film 10 which fills the convexities presented by the TFT and the color filter 9 so as to provide a flat smooth surface." However, the color filters shown in Fig. 1 have concavities and convexities, and thus do not have flattened surfaces. Additionally, the quoted sentence should be understood as indicating that the TFT and the color

filters cause the convexities, and the planarization film takes a roll of flattening the convexities. Accordingly, applicant submits that neither Kadota et al., nor any of the other cited references, teach a color filter having a flattened surface. Thus, applicant submits that independent claims 46-48, 50, 52 and 54, the claims that are dependent therefrom, are patentable over the art of record.

Turning to independent claims 56-58, 60 and 61, these claims require that the color filter be formed over the passivation film or the interlayer insulating film and the first thin film transistor. The color filter shown in Kadota et al. apparently does not cover the TFT's, and the other cited references do not seem teach a color filter covering a passivation film and a TFT. Accordingly, applicant submits that claims 56-58, 60 and 61, and the claims dependent therefrom, are patentable over the art of record.

Based upon the foregoing, applicant believes that the application is now in condition for allowance and an early Office Action in this regard is earnestly solicited.

Respectfully submitted,

Dated: February 3, 2004

Stephen B. Heller

Stephen B. Heller
Attorney of Record
Registration No.: 30,181
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PTO/SB/30 (10-01)
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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Address to:
Commissioner for Patents
Box RCE
Washington, DC 20231

Application Number	09/516,028
Filing Date	March 1, 2000
First Named Inventor	Satoshi Murakami
Art Unit	2815
Examiner Name	Eugene Lee
Attorney Docket Number	0553-0163

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114

a. ☐ Previously submitted
   i. ☐ Consider the amendment(s)/reply under 37 CFR 1.116 previously filed on _____
   (Any unentered amendment(s) referred to above will be entered).
   ii. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
   iii. ☐ Other _____

b. ☒ Enclosed
   i. ☒ Amendment/Reply
   ii. ☐ Affidavit(s)/Declaration(s)
   iii. ☒ Information Disclosure Statement (IDS)
   iv. ☐ Other _____

2. Miscellaneous

a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

b. ☐ Other _____

3. Fees — The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

a. ☒ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. 50-1039
   i. ☒ RCE fee required under 37 CFR 1.17(e)
   ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)
   iii. ☐ Other _____

b. ☒ Check in the amount of $ 1,958.00 enclosed

c. ☐ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print/Type)	Stephen B. Heller	*Registration No. (Attorney/Agent)*	30,181
Signature	Stephen B. Heller	*Date*	February 3, 2004

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner For Patents, Box RCE, Washington, DC 20231, or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Name (Print/Type)	Kristine Callahan		
Signature	Kristine Callahan	*Date*	February 3, 2004

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND Fees and Completed Forms to the following address: Assistant Commissioner for Patents, Box RCE, Washington, DC 20231.

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Sheet 1 of 1

Complete if Known	
Application Number	09/516,028
Filing Date	March 1, 2000
First Named Inventor	Satoshi Murakami
Art Unit	2815
Examiner Name	Eugene Lee
Attorney Docket Number	0553-0163

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US- 2001/0025958	10/4/2001	Yamazaki et al.	
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FOREIGN PATENT DOCUMENTS

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	2	JP 328000/1996	12/13/1996	Semiconductor		X

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RE: APPLICATION ATTY/SEC: SBH/KLC
File no: 0553-0163
Applicant: SATOSHI MURAKAMI
09/516,082 ⇒
S.N.: 09/516,028 Filing Date: 3/1/2000
Title: SEMICONDUCTOR DEVICE + METHOD OF MANUFACTURING THE SAME
Due date: _____ Date Sent: 2/3/2004

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